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(54) A data input and output control device and a one-chip microcomputer integrating the same

Steuereinrichtung für Daten-Ein-/Ausgang und diese beinhaltender Ein-Chip-Mikrocomputer

Dispositif de contrôle d'entrée/sortie de données et un micro-ordinateur monopuce intégrant le même

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- **PATENT ABSTRACTS OF JAPAN vol. 15, no. 251 (P-1220)26 June 1991 & JP-A-30 081 851 (SEIKO) 8 April 1991**
- **PATENT ABSTRACTS OF JAPAN vol. 9, no. 257 (P-396)15 October 1985 & JP-A-60 107 168 (NIPPON DENKI) 12 June 1985**

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EP 0 549 334 B1

Description

BACKGROUND OF THE INVENTION

(1) Field of the Invention

[0001] This invention relates to a serial interface embedded in a one-chip LSI together with a processor; particularly to an improvement in a data input/output control device for a transfer of data between the processor and an external apparatus and another improvement in a one-chip microcomputer.

(2) Description of the Related Art

[0002] Conventionally, the serial interface embedded in the one-chip LSI together with the processor is operated at a processor clock for the processor when the transfer of data is conducted between the processor and the external apparatus, such as by synchronizing a signal inputted to the serial interface (a data transfer clock and signals necessary for the transfer of the data from the external apparatus) with the processor clock.

[0003] The conventional serial interface is described hereunder with referring to drawings.

[0004] A construction of the conventional serial interface, the processor and the external apparatus are shown in FIG. 1. As shown in the figure, the serial interface is equipped with a data input/output control device and an input/output data transfer device, the former comprising all the units except 530, 540 and 550 while the latter comprising 530, 540, and 550.

[0005] Data are outputted from or inputted to an external apparatus 500, and a transmission or a reception of the data is conducted between the external apparatus 500 and the embedded-type serial interface equipped with the devices referred to as numeral references above 500.

[0006] A transfer clock 501 is supplied from the external apparatus 500.

[0007] A transfer control signal 502 shows that the transfer of the data to the external apparatus is ready.

[0008] A processor 503 stores the data inputted from the external apparatus 500 or executes an operation.

[0009] A processor clock 504 is for an operation of the processor 503.

[0010] A controller 510 outputs control signals, which is synchronized with the processor clock 504.

[0011] A ready signal 511 is outputted from the controller 510 to show that the input or the output of the data is ready.

[0012] A synchronization means 521 synchronizes the transfer clock 501 with the processor clock 504, which is shown in a time chart of FIG. 2.

[0013] A synchronization means 522 synchronizes the transfer control signal 502 with the processor clock 504, which is shown in a time chart of FIG. 3.

[0014] A clock 523 is synchronized with the processor clock 504 by the synchronization means 521.

[0015] A signal 524 is outputted from the synchronization means 522.

[0016] An output buffer 530 holds the data of n bits (n is a positive integer) transferred from the processor 503 to the external apparatus 500.

[0017] A shift register 540 obtains the data of n bits outputted from the output buffer 530, which is synchronized with the clock 523 in accordance with a transmission data load signal outputted from the controller 510. The shift register 540 shifts the data in a direction of the most significant bit (MSB) by one bit at one time, which is synchronized with the clock 523 in accordance with a shift clock signal.

[0018] One-bit data 541 located at the MSB of the shift register 540 are outputted to the external apparatus 500.

[0019] One-bit data 542 from the external apparatus 500 are inputted to the least significant bit (LSB) of the shift register 540.

[0020] An input buffer 550 obtains the data of n bits held in the shift register 540, which is synchronized with the processor clock 504 in accordance with the shift clock signal outputted from the controller 510.

[0021] A down counter 560 is set with an initial number m ($0<m\leq n$; m is an integer) for a start of a count down of the bits in the data to be inputted or outputted, and reduces m by one at a timing of the clock 523.

[0022] A flag circuit 570 with a flag showing statuses of the output buffer 530 and the input buffer 550 is set with a set signal 571 outputted from the controller 510 and is reset with a reset signal 572 outputted from the processor 503, the set signal 571 and the reset signal 572 being synchronized with the processor clock 504.

[0023] The serial interface constructed the above is operated to output the data or input the data; the operations are described hereunder with referring to FIGs. 1, 2, and 3 (refer to "MN 19011, 1909 LSI Manual" by Matsushita Electronics Corporation).

[output of the data]

[0024] The processor 503 writes in the output buffer 530 the data to be outputted to the external apparatus 500, and resets the flag circuit 570 with the reset signal 572 so that the controller 510 is informed that the data are held in the output buffer 530.

[0025] When a flag is reset, the controller 510 outputs the control signal 511 of 1 to inform the external apparatus 500 that output of the data is ready. Detecting the control signal 511 of 1, the external apparatus 500 outputs the control signal 502 of 1. An alternation timing of the transfer control signal 502 is synchronized with the processor clock 504 by the synchronization means 522 to be outputted as the signal 524. The signal 524 is then inputted to the controller 510.

[0026] When the signal 524 is 1, the controller 510 outputs a transmission data load signal so that the data are transferred from the output buffer 530 to the shift

register 540. Simultaneously, the controller 510 outputs a load signal so that the initial number m is set to the down counter 560. The first one-bit data 541 located at the MSB of the shift register 540 are transferred to the external apparatus 500. Simultaneously, the controller 510 sets the flag circuit 570 with the set signal 571.

[0027] The controller 510 refers to the signal 524. If the signal 524 holds 1, the controller 510 outputs a shift clock signal so that the data in the shift register 540 are shifted in the direction of the MSB by one bit at a falling edge of the clock 523, and the second one-bit data 541 located next to the MSB are outputted. Simultaneously the controller 510 outputs a count clock signal so that a number m-1, obtained by reducing the initial number m by one, is held by the down counter 560.

[0028] If the signal 524 is 0, the controller 510 does not output the shift clock signal so that the shift register 540 is not operated.

[0029] The above operations are repeated until (m+1) th data are outputted (until the down counter 560 counts 0).

[0030] When the above operations are conducted, the processor 503 refers to the flag circuit 570. If the flag circuit 570 is reset to show that the data are in the output buffer 530, the processor 503 does not write data into the output buffer 530. If the flag circuit 570 is set, the processor 503 writes data in the output buffer 530 and resets the flag circuit 570. Hence, the processor 503 writes in the output buffer 530 all the data to be outputted, one by one.

[0031] When the down counter counts 0, the controller 510 refers to the flag circuit 570. If the flag circuit 570 is reset to show that the data are in the output buffer 530, the controller 510 outputs the transmission data load signal so that the data in the output buffer 530 are transferred to the shift register 540, and sets the flag circuit 570 with the set signal 571. Simultaneously, the controller 510 outputs the load signal so that the initial number m is set to the down counter 560. If the flag circuit 570 is set to show that no data are in the output buffer 530, the controller 510 outputs 0 of the ready signal 511 so that the external apparatus 500 is informed that the output of the data is completed.

[input of the data]

[0032] The processor 503 reads the data in the input buffer 550 and then resets the flag circuit 570 with the reset signal 572 to show that no data are held in the input buffer 550.

[0033] Informed that the flag circuit 570 is reset, the controller 510 outputs 1 of the ready signal 511 to show that the data are ready to be inputted. Detecting the ready signal 511 of 1, the external apparatus 500 outputs 1 of the transfer control signal 502. An alternation timing of the transfer control signal 502 is synchronized with the processor clock 504 by the synchronization means 522 to be outputted as the signal 524.

[0034] Detecting the signal 524 of 1, the controller 510 outputs a reception data load signal to the input buffer 550 so that the data in the shift register 540 (the data which has been inputted thereto) are copied, and first one-bit data 542 are outputted from the external apparatus 500 at a rising edge of the transfer clock 501. Simultaneously the controller 510 outputs the load signal so that the initial number m is set to the down counter.

[0035] The controller 510 refers to the signal 524. If the signal 524 holds 1, the controller 510 outputs the shift clock signal to the shift register 540 so that the data in the shift register 540 are shifted in the direction of the MSB by one bit, and the first one-bit data 542 are inputted to the LSB of the shift register 540 at the timing of the clock 523. Simultaneously the controller outputs the count clock signal so that the number m-1 is held by the down counter 560. If the signal 524 is 0, the controller 510 does not output the count clock signal so that the shift register 540 is not operated.

[0036] The operations described the above are repeated until the (m+1)th data are inputted (the down counter 560 counts 0).

[0037] When the above operations are conducted, the processor 503 refers to the flag circuit 570. If the flag circuit 570 is reset to show that no data are in the input buffer 550, the processor 503 does not read any data therefrom. If the flag circuit 570 is set to show that the data are held in the input buffer 550, the processor 503 reads the data and resets the flag circuit 570.

[0038] When the down counter 560 counts 0, the controller 510 refers to the flag circuit 570. If the flag circuit 570 is reset to show that the data in the input buffer 550 have been read, the controller 510 outputs the reception data load signal so that the data in the shift register 540 are transferred to the input buffer 550, and sets the flag circuit 570. Simultaneously the initial number m is set to the down counter 560.

[0039] If the flag circuit 570 is set to show that the data in the input buffer 550 have not been read by the processor 503, the controller 510 outputs 0 of the ready signal 511 so that the external apparatus 500 is informed that the input of the data is not ready.

[0040] As is described hereinbefore, the embedded-type serial interface synchronizes, at the input of the data, the data transfer clock and the signals necessary for the transfer of the data with the processor clock 504 for the processor 503. Such synchronization enables the serial interface to conduct the operations based on the processor clock 504 for the processor 503.

[0041] However, since all the units composing the whole serial interface are synchronized with the processor clock 504 for the processor 503, a loss of electric power has been observed. That is, a commonly utilized processor clock frequency is several tens of Mega Hertz (MHz) and this is much higher than a frequency required for the input and the output of data, that is several tens of kilo Hertz (kHz). It is commonly known that the higher the frequency required for the device is, the more the

electric power consumed thereby is. Particularly when a circuit is designed by utilising a CMOS type transistor, an amount of electric power consumed at the circuit increases along with an increase in the processor clock frequency thereof.

[0042] A conventional serial data transfer system is described in European patent application EP-A-0 258 872. The timing of serial communications between master and slave processors is carried out by use of a dedicated clock line which can be driven by the selected master processor's serial clock source. The external clock pulses are used to control the handshaking and data transfer timing but there is no appreciation of the problems of synchronisation between the operation of the processor and the data input output control device. In Japanese patent application JP-A-3 081 851, serial communication is speeded up by providing dual port RAMs on coprocessors including serial communication ports using an interface with a CPU. Whilst the setting of status flags is described, the problem of synchronisation between the operation of the CPU and the coprocessors of the data input output control device is not appreciated.

SUMMARY OF THE INVENTION

[0043] It is a primary object of the present invention to provide the data input/output control device in the serial interface which eliminates the loss of electric power, which is caused by a difference between the processor clock frequency and the frequency required for the data input and the data output even when the processor clock frequency is extremely high, and the one-chip microcomputer utilising such device.

[0044] According to the present invention there is provided a data input/output control device integrated in a one-chip microcomputer together with a data transfer device and a processor, the data transfer device being arranged to transmit to and receive from an external apparatus serial data and the processor processing data inputted to the data transfer device and transmitting the processed data to the data transfer device to be further transmitted to the external apparatus, the data input/output control device comprising: a controller for controlling the data input and the data output of said data transfer device; and a flag holding unit for holding a flag which shows if the data have been inputted to the data transfer device by one of the processor and the external apparatus characterised in that: a clock of the data input/output control device for an operation thereof is a transfer clock utilised by the external apparatus and the transfer clock is slower than a clock for the processor; and in that the data input/output control device further comprises: a first synchronisation circuit for synchronising an output from the flag holding unit with the transfer clock, the output being sent to the controller; and a second synchronisation circuit for synchronising the output from the flag holding unit with the clock for the processor.

[0045] The data transfer device may comprise a shift register for converting a transmission data from parallel into serial and a reception data from serial into parallel, a reception buffer for holding temporarily the data which have been stored in the shift register so that they are inputted to the processor, and a transmission buffer for holding temporarily the data outputted from the processor so that they are stored in the shift register, wherein the flag holding unit holds the flag which shows if the transmission buffer holds the data at a transmission of the data as well as shows if the reception buffer holds the data at a reception of the data.

[0046] The controller may be constructed to control the shift register for transmitting to and receiving from the external apparatus the serial data, wherein the controller may be arranged at the transmission of the data, to transfer the data in the transmission buffer to the shift register and to output a shift clock to the shift register so that the serial data are transmitted if said flag shows that the transmission buffer holds the data, and at the reception of the data, to output the shift clock to the shift register in order to obtain the serial data outputted from the external apparatus, to transfer the reception data in the shift register to the reception buffer, and to change the flag in the flag holding unit to show that the reception data are in the reception buffer.

[0047] The controller may comprise a transmission control circuit for outputting a load signal so that the shift register is loaded with the transmission data when the flag shows that the transmission buffer holds the data at the transmission of the data, a shift clock output circuit for outputting the shift clock to the shift register when the shift register is loaded with the transmission data at the transmission of the data as well as outputting the shift clock to the shift register when a transfer ready signal is outputted from the external apparatus thereto at the reception of the data, and a reception control circuit for obtaining the reception data from the shift register and changing the flag in the flag holding unit to show that the reception data are held therein.

[0048] The data input/output control device may further comprise a counter for counting the number of bits in the data to be transferred when the serial data are transferred therefrom to the external apparatus as well as the serial data are transferred from the external apparatus thereto.

[0049] The data input/output control device constructed as above utilizes as a clock the transfer clock generated by the external apparatus in order to control the input and the output of the data transfer device, the transfer clock being slower than the processor clock for the processor.

[0050] Therefore, according to the data input/output control 15 device and the one-chip microcomputer of the present invention, the loss of electric power which is caused by the difference between the processor clock frequency and the frequency required for the data input and the data output is eliminated; therefore, power dis-

sipation required for the data transfer of the conventional data input/output control device can be reduced even when the processor clock frequency for the processor is extremely high. Particularly when the CMOS type device is utilized, such effect is significant.

[0051] Also conventionally a certain amount of electricity is consumed regardless of conditions including a transfer speed, which varies depending on a kind of the external apparatus, and
a presence/an absence of the external apparatus. However the data input/output control device of the present invention is constructed to consume different amounts of electricity in accordance with the transfer clock, and this increases energy efficiency.

BRIEF DESCRIPTION OF THE DRAWINGS

[0052] These and other objects, advantages and features of the invention will become apparent from the following description thereof taken in conjunction with the accompanying drawings which illustrate a specific embodiment of the invention. In the drawings:

[0053] FIG. 1 is an illustration showing a construction of the conventional serial interface, the processor, and the external apparatus.

[0054] FIG. 2 is a time chart of the clocks utilized by the conventional data input/output device.

[0055] FIG. 3 is a time chart of the control signals utilized by the conventional data input/output device.

[0056] FIG. 4 is an illustration showing a construction of a serial interface, the processor, and the external apparatus, all of which are in the embodiment of the present invention.

[0057] FIG. 5 is an illustration showing a construction of the shift register in the embodiment of the present invention.

[0058] FIG. 6 is an illustration showing a construction of a controller in the embodiment of the present invention.

[0059] FIG. 7 is a time chart of timings utilized for an output of data in the embodiment of the present invention.

[0060] FIG. 8 is a time chart of timings utilized for an input of data in the embodiment of the present invention.

DETAILED DESCRIPTION OF THE EMBODIMENT

[0061] A construction of a serial interface, a processor and an external apparatus are shown in FIG. 4. As shown in the figure, the serial interface is equipped with a data input/output data control device 10 and a data transfer device 11, the former comprising all the units except 130, 140 and 150, while the latter comprising 130, 140, and 150.

[0062] Data are outputted from or inputted to an external apparatus 100 such as an A/D converter and other processors.

[0063] A transfer clock signal 101 is supplied from the external apparatus 100.

[0064] A transfer control signal 102 shows that a transfer of the data to the external apparatus 100 is ready.

[0065] A processor 103 reads the data in an input buffer 150, writes the data into an output buffer 130, refers to or resets a flag circuit 170, and executes other operations and processings.

[0066] A processor clock 104 is for an operation of the processor 103.

[0067] A controller 110 outputs control signals to control the embedded-type data input/output control device 10, which is synchronized with the transfer clock signal 101.

[0068] A ready signal 111 is outputted from the controller 110 to show that the input or the output of the data is ready.

[0069] An output buffer 130 holds the data of n bits (n is a positive integer, for example, 24) to be outputted from the processor 103 to the external apparatus 100.

[0070] A shift register 140 obtains the data of n bits outputted from the output buffer 130, which is synchronized with the transfer clock signal 101 in accordance with a transmission data load signal outputted from the controller 110. The shift register 140 shifts the data in a direction of the most significant bit (MSB) by one bit at one time, which is synchronized with the transfer clock signal 101 in accordance with a shift clock signal.

[0071] A construction of the shift register 140 is described hereunder with referring to FIG. 5. As shown in the figure, the shift register 140 comprises a shifter 200 and a latch circuit 201. The shifter 200 is loaded with the data outputted from the output buffer 130 when a transmission data load signal 212 becomes active, then holds one-bit data located at a S_{in} terminal (the least significant bit, LSB, side), shifts the data in a direction of the MSB at a falling edge of the shift clock signal 211, and outputs one-bit data located at the MSB from a S_{out} terminal (the MSB side). The latch circuit 201 latches the data shifted out by the shifter 200 and outputs the data at a rising edge of the shift clock signal. That is, transmission data are outputted from the latch circuit 201 at the rising edge while reception data are inputted to the shifter 200 at the falling edge. Hereinafter it is assumed that the shift register 140 shifts the transmission data at the rising edge of the shift clock signal and shifts the reception data at the falling edge thereof.

[0072] One-bit data 141 located at the MSB of the shift register 140 are outputted to the external apparatus 100.

[0073] One-bit data 142 are transferred from the external apparatus 100 to the LSB of the shift register 140.

[0074] An input buffer 150 obtains the data of n bits held in the shift register 140, which is synchronized with the transfer clock signal 101 in accordance with the shift clock signal outputted from the controller 110.

[0075] A down counter 160 is set with an initial number m ($0<m\leq n$; m is an integral number) for a start of a count down of the bits in the data, and reduces m

by one in accordance with a count clock signal outputted from the controller 110.

[0076] A flag circuit 170 is set with a flag set signal 171 outputted from the controller 110 and is reset with a flag reset signal 172 outputted from the processor 103, the flag set signal 171 being synchronized with the transfer clock signal 101 and the flag reset signal 172 being synchronized with the processor clock 104.

[0077] A synchronization means 181 synchronizes an alternation timing of the flag circuit 170 with the transfer clock signal 101.

[0078] A synchronization means 182 synchronizes the alternation timing of the flag circuit 170 with the processor clock 104.

[0079] A flag signal 183 is outputted from the flag circuit 170 via the synchronization means 181.

[0080] A construction of the controller 110 is described hereunder with referring to FIG. 6.

[0081] A terminal count signal 112 is outputted from the down counter 160 when it counts 0.

[0082] A reception data load signal 113 transfers the data in the shift register 140 to the input buffer 150.

[0083] A shift clock/count clock signal 211 orders a shift of the shift register 140 or a counting of the down counter 160.

[0084] A transmission data load/initial number load signal 212 orders a transfer of the data from the output buffer 130 to the shift register 140 or a load of the number to be counted down by the down counter 160.

[0085] A state transition control circuit 301 controls the data input/output control device 10 and the data transfer device 11 depending on a state of the data transferred between the device 11, the processor 103, and the external apparatus 100.

[0086] An AND circuit 302 outputs the transfer clock signal 101 as the shift clock/count clock signal 211 when the transfer control signal 102 and the ready signal 111 becomes active.

[0087] An input buffer control circuit 303 activates the transmission data load/initial number load signal 212 so that the input buffer 150 is loaded with the data in the shift register 140 when the flag signal 183 is 0 and the down counter 160 counts 0 at the reception of data, the activation being synchronized with the transfer clock signal 101.

[0088] The serial interface constructed the above is operated to output the data or input the data; the operations are described hereunder with referring to the drawings.

[output of the data]

[0089] The processor 103 writes in the output buffer 130 the data to be outputted to the external apparatus 100 and resets the flag circuit 170 with the flag reset signal 172 so that the controller 110 is informed that the data are held in the output buffer 130. The output signal of the flag circuit 170 is synchronized with the transfer clock signal 101 by the synchronization means 181 to be outputted as the flag signal 183. The flag signal 183 is then inputted to the state transition control circuit 301 in FIG. 6 and is sampled thereby at a falling edge of the transfer clock signal 101. Then the state transition control circuit 301 refers to the flag signal 183. If the flag signal 183 is 0, the state transition control circuit 301 outputs 1 of the ready signal 111 so that the external apparatus 100 is informed that the transmission of the data is ready. Detecting the ready signal 111 of 1, the external apparatus 100 outputs 1 of the transfer control signal 102 to show that the reception of the data is ready.

[0090] Detecting the transfer control signal 102 of 1, the state transition control circuit 301 activates the transmission data load/initial number load signal 212. Directed by the signal 212, the data are transferred from the output buffer 130 to the shift register 140 at the rising edge of the transfer clock signal 101 shown by (p) in FIG. 7 (FIG. 7 is a reference for timings of output executions), and the first one-bit data 141 are outputted to the external apparatus 100. Simultaneously, the initial number is set to the down counter 160, and the flag circuit 170 is set with the flag set signal 171 to show that the output buffer 130 is ready to receive new data.

[0091] The state transition control circuit 301 refers to the transfer control signal 102. If the transfer control signal 102 holds 1, the state transition control circuit 301 outputs the shift clock/count clock signal 211, which is executed at (b) timing in the figure. Directed by the signal 211, the data in the shift register 140 are shifted in a direction of the MSB by one bit at the rising edge of the transfer clock signal 101, shown by (q) in the figure, and the second one-bit data 141 are outputted. Simultaneously a number m-1, obtained by reducing the initial number m by one, is held by the down counter 160. If the transfer control signal 102 is 0, the state transition control circuit 301 does not output the shift clock/counter clock signal 211 so that the shift register 140 is not operated. The above operations are repeated until (m+1) th data are outputted (until the down counter 160 counts 0).

[0092] Inputted with the terminal count signal 112, the state transition control circuit 301 refers to the flag circuit 170. If the flag circuit 170 is reset to show that the data are in the output buffer 130, the state transition control circuit 301 activates the transmission data load/initial number load signal 212 so that the data in the output buffer 130 are transferred to the shift register 140, and sets the flag circuit 170 with the flag set signal 171. Simultaneously the initial number m is set to the down counter 160. If the flag circuit 170 is set to show that no data are in the output buffer 130, the state transition control circuit 301 outputs 0 of the ready signal 111 so that the external apparatus is informed that the output of the data is completed, which is executed at (c) in the figure.

[0093] The processor 103 refers to a status of the flag circuit 170 via the synchronization means 182. If the flag circuit 170 is reset to show that data are in the output

buffer 130, the processor 103 does not write any data into the output buffer 130. If the flag circuit 170 is set, the processor 103 writes data into the output buffer 130 and resets the flag circuit 170.

[input of the data]

[0094] The processor 103 reads the data in the input buffer 150 and then resets the flag circuit 170 with the reset signal 172 outputted at the timing of the processor clock 104 to show that no data are held in the input buffer 150.

[0095] Informed via the synchronization means 181 that the flag circuit 170 is reset at the rising edge of the transfer clock signal 101, the state transition control circuit 301 outputs 1 of the ready signal 111 to show that the data are ready to be inputted, which is executed at (a) timing in FIG. 8. (FIG. 8 is a reference for timings of input executions). Detecting the ready signal 111 of 1, the external apparatus 100 outputs the first one-bit data 142 at the rising edge of the transfer clock signal 101, and then outputs 1 of the transfer control signal 102.

[0096] Detecting the transfer control signal 102 of 1, the state transition control circuit 301 outputs the shift clock signal/count clock signal 211 and activates the transmission data load/number load signal 212, which are executed at (b) in the figure. Directed by the signals 211 and 212, the data in the shift register 140 are shifted in the direction of the MSB by one bit at the falling edge of the transfer clock signal 101, which is shown by (p) in the figure, and the first one-bit data 142 are inputted to the LSB of the shift register 140. Simultaneously the initial number m is set to the down counter 160 at the falling edge of the transfer clock signal 101, shown by (p) in the figure.

[0097] The state transition control circuit 301 refers to the transfer control signal 102. If the transfer control signal 102 holds 1, the state transition control circuit 301 outputs the shift clock/count clock signal 211, which is executed at (c) in the figure. Directed by the signal 211, the shift register 140 shifts the data in a direction of the MSB by one bit at the falling edge of the transfer clock signal 101, shown by (q) in the figure, and the down counter 160 holds the number m-1 at the falling edge of the transfer clock signal 101, shown by (q) in the figure. If the transfer control signal 102 is 0, the state transition control circuit 301 does not output the shift clock/count clock signal 211 so that the shift register 140 is not operated.

[0098] The operations described the above are repeated until the (m+1)th data are inputted (the down counter 160 counts 0).

[0099] Inputted with the terminal count signal 112 at the rising edge of the transfer clock signal 101, the controller 110 refers to the status of the flag circuit 170. If the flag circuit 170 is reset to show that no data are in the input buffer 150, the controller 110 outputs the reception data load signal 113 so that the data in the shift register 140 are transferred to the input buffer 150, and sets the flag circuit 170. Simultaneously the controller 110 outputs the transmission data load/initial number load signal 212 to the down counter 160 so that the initial number m is set to the down counter 160.

[0100] If the flag circuit is set to show that the data in the input buffer 150 have not been read by the processor 103, the controller 110 outputs 0 of the ready signal 111 so that the external apparatus 100 is informed that the input of the data is completed.

[0101] The processor 103 refers to a status of the flag circuit 170 via the synchronization means 182. If the flag circuit 170 is reset to show no data are in the input buffer 150, the processor 103 does not read data therefrom. If the flag circuit 170 is set to show new data are held in the input buffer, the processor 103 reads the data and resets the flag circuit 170.

[0102] The input and output of the data may utilize other devices or methods instead of the reference of the flag circuit which reflects the statuses of the input and the output buffers.

[0103] Although the present invention has been fully described by way of examples with reference to the accompanying drawings, it is to be noted that various changes and modifications will be apparent to those skilled in the art.

Claims

1. A data input/output control device (10) integrated in a one-chip microcomputer together with a data transfer device (11) and a processor (103), the data transfer device (11) being arranged to transmit to and receive from an external apparatus (100) serial data and the processor (103) processing data inputted to the data transfer device (11) and transmitting the processed data to the data transfer device (11) to be further transmitted to the external apparatus (100), the data input/output control device (10) comprising: a controller (110) for controlling the data input and the data output of said data transfer device (11); and a flag holding unit (170) for holding a flag which shows if the data have been inputted to the data transfer device (11) by one of the processor (103) and the external apparatus (100) characterised in that:

   a clock of the data input/output control device (10) for an operation thereof is a transfer clock utilised by the external apparatus (100) and the transfer clock (101) is slower than a clock (104) for the processor (103); and in that the data input/output control device (10) further comprises:

   a first synchronisation circuit (181) for synchronising an output from the flag holding unit (170) with the transfer clock (101), the output being sent to the controller (110); and

a second synchronisation circuit (182) for synchronising the output from the flag holding unit (170) with the clock (104) for the processor (103).

2. The data input/output control device (10) of claim 1, wherein the data transfer device (11) comprises:

a shift register (140) for converting transmission data from a parallel into a serial format and reception data from a serial into a parallel format;
a reception buffer (150) for temporarily holding the data which have been stored in the shift register (140) so that they can be input to the processor (103); and
a transmission buffer (130) for holding temporarily the data output from the processor (103) so that they can be stored in the shift register (140),

wherein the flag holding unit (170) holds the flag which shows if the transmission buffer (130) holds the data at a transmission of the data and also shows if the reception buffer (150) holds the data at a reception of the data.

3. The data input/output control device (10) of claim 2, wherein the controller (110) is arranged to control the shift register (140) for transmitting to and receiving from the external apparatus (100) the serial data, wherein the controller (110) is arranged:

at the transmission of the data, to transfer the data in the transmission buffer (130) to the shift register (140) and to output a shift clock (101,211) to the shift register (140) so that the serial data are transmitted if said flag shows that the transmission buffer (130) holds the data; and
at the reception of the data, to output the shift clock (101,211) to the shift register (140) in order to obtain the serial data output from the external apparatus (100), to transfer the reception data in the shift register (140) to the reception buffer (130), and to change the flag in the flag holding unit (170) to show that the reception data are in the reception buffer (150).

4. The data input/output control device (10) of claim 3, wherein the controller (110) comprises:

a transmission control circuit (301) for outputting a load signal (212) so that the shift register (140) is loaded with the transmission data when said flag shows that the transmission buffer (130) holds the data at the transmission of the data;
a shift clock output circuit (302) for outputting the shift clock (101,211) to the shift register (140) when the shift register (140) is loaded with the transmission data at the transmission of the data as well as outputting the shift clock (101,211) to the shift register (140) when a transfer ready signal is output from the external apparatus (100) thereto at the reception of the data; and
a reception control circuit (303) for obtaining the reception data from the shift register (140) and changing the flag in said flag holding unit (170) to show that the reception data are held therein.

5. The data input/output control device (10) of any preceding claim, further comprising a counter (160) for counting the number of bits in the data to be transferred therefrom to the external apparatus (100) as well as the serial data are transferred from the external apparatus (100) thereto.

Patentansprüche

1. Daten-Eingabe/Ausgabe-Steuergerät (10), das zusammen mit einem Daten-Übertragungsgerät (11) und einem Prozessor (103) in einem Ein-Chip-Microcomputer integriert ist, wobei das Daten-Übertragungsgerät (11) ausgelegt ist, serielle Daten an eine externe Vorrichtung (100) zu senden und von ihr zu empfangen, und der Prozessor (103) dem Daten-Übertragungsgerät (11) eingegebene Daten verarbeitet und die verarbeiteten Daten zu dem Daten-Übertragungsgerät (11) zum weiteren Übertragen zu der externen Vorrichtung (100) überträgt, und das Daten-Eingabe/Ausgabe-Steuergerät (10) umfaßt: eine Steuerung (110) zum Steuern der Dateneingabe und der Datenausgabe des Daten-Übertragungsgerätes (11); und eine Merker-Halteeinheit (170), um einen Merker zu halten, welcher zeigt, ob die Daten durch eines der Geräte, Prozessor (103) oder externe Vorrichtung (100), dem Daten-Übertragungsgerät (11) eingegeben wurden, **dadurch gekennzeichnet, daß**:

ein Takt des Daten-Eingabe/Ausgabe-Steuergerätes (10) für einen Betrieb desselben ein Übertragungstakt ist, der von der externen Vorrichtung (100) benützt wird, und der Übertragungstakt (101) langsamer als ein Takt (104) für den Prozessor (103) ist; und daß das Daten-Eingabe/Ausgabe-Steuergerät (10) weiter umfaßt:

eine erste Synchronisations-Schaltung (181) zum Synchronisieren einer Ausgabe von der Merker-Halteeinheit (170) mit dem Übertragungstakt (101), wobei die Ausgabe zu der Steuerung (110) gesendet wird; und

eine zweite Synchronisations-Schaltung (182) zum Synchronisieren der Ausgabe von der Merker-Halteeinheit (170) mit dem Takt (104) für den Prozessor (103).

2. Daten-Eingabe/Ausgabe-Steuergerät (10) nach Anspruch 1, bei dem das Daten-Übertragungsgerät (11) umfaßt:

ein Schieberegister (140), um Übertragungsdaten von einem parallelen in ein serielles Format und Empfangsdaten von einem seriellen in ein paralleles Format zu wandeln;
einen Empfangspuffer (150) zum zeitweiligen Halten der Daten, welche in dem Schieberegister (120) gespeichert wurden, so daß sie zu dem Prozessor (103) eingegeben werden können; und
einen Übertragungspuffer (130) zum zeitweiligen Halten der Ausgabedaten von dem Prozessor (103), so daß sie in dem Schieberegister (140) gespeichert werden können,
wobei die Merker-Halteeinheit (170) den Merker hält, der zeigt, ob der Übertragungspuffer (130) die Daten bei einer Übertragung der Daten hält, und auch zeigt, ob der Empfangspuffer (150) die Daten bei einem Empfang der Daten hält.

3. Daten-Eingabe/Ausgabe-Steuergerät (10) nach Anspruch 2, bei dem die Steuerung (110) ausgelegt ist, das Schieberegister (140) zum Senden der seriellen Daten zu der externen Vorrichtung (100) und zum Empfangen von der externen Vorrichtung (100) zu steuern, wobei die Steuerung (110) ausgelegt ist:

bei der Übertragung der Daten, die Daten in den Übertragungspuffer (130) zu dem Schieberegister (140) zu übertragen und einen Schiebetakt (101, 211) so zu dem Schieberegister (140) auszugeben, daß die seriellen Daten übertragen werden, wenn der Merker zeigt, daß der Übertragungspuffer (130) die Daten hält; und
beim Empfang der Daten den Schiebetakt (101, 211) zu dem Schieberegister (140) auszugeben, um die von der externen Vorrichtung (100) ausgegebenen seriellen Daten zu erhalten, die Empfangsdaten in dem Schieberegister (140) zu dem Aufnahmepuffer (130) zu übertragen und den Merker in der Merker-Halteeinheit (170) so zu ändern, daß er zeigt, daß die Aufnahmedaten sich in dem Aufnahmepuffer (150) befinden.

4. Daten-Eingabe/Ausgabe-Steuergerät (10) nach Anspruch 3, bei dem die Steuerung (110) umfaßt:

eine Übertragungs Steuerschaltung (301), um ein Ladesignal (212) so auszugeben, daß das Schieberegister (140) mit den Übertragungsdaten beladen wird, wenn der Merker zeigt, daß der Übertragungspuffer (130) die Daten bei der Übertragung der Daten hält;
eine Schiebetakt-Ausgabeschaltung (302) zum Ausgeben des Schiebetaktes (101, 211) an das Schieberegister (140), wenn das Schieberegister bei der Übertragung der Daten mit den Übertragungsdaten geladen wird, wie auch zum Ausgeben des Schiebetaktes (101, 211) zu dem Schieberegister (140), wenn ein Übertragungs-Bereit-Signal von der externen Vorrichtung (100) dazu bei dem Empfang der Daten ausgegeben wird; und
eine Aufnahme-Steuerschaltung (303) zum Aufnehmen der Empfangsdaten von dem Schieberegister (140) und Ändern des Merkers in der Merker-Halteeinheit (170), um zu zeigen, daß die Empfangsdaten darin gehalten werden.

5. Daten-Eingabe/Ausgabe-Steuergerät (10) nach einem der vorangehenden Ansprüche, das weiter einen Zähler (160) enthält, um die Bitzahl in den davon zu der externen Vorrichtung (100) zu übertragenden Daten zu zählen, wie auch die der seriellen Daten, die von der externen Vorrichtung (100) dazu übertragen werden.

Revendications

1. Dispositif de gestion d'entrées/sorties de données (10) intégré dans un micro-ordinateur monopuce ensemble avec un dispositif de transfert de données (11) et un processeur (103), le dispositif de transfert de données (11) étant arrangé pour transmettre à et recevoir à partir d'un appareil externe (100) des données en série et le processeur (103) traitant les données entrées dans le dispositif de transfert de données (11) et transmettant les données traitées au dispositif de transfert de données (11) pour être ensuite transmises à l'appareil externe (100), le dispositif de gestion d'entrées/sorties de données (10) comprenant : un contrôleur (110) pour contrôler l'entrée de données et la sortie de données dudit dispositif de transfert de données (11) ; et une unité de maintien d'indicateurs (170) pour maintenir un indicateur qui montre si les données ont été entrées dans le dispositif de transfert de données (11) par le processeur (103) ou l'appareil externe (100), caractérisé en ce que :

une horloge du dispositif de gestion d'entrées/sorties de données (10) pour son fonctionnement est une horloge de transfert utilisée par l'appareil externe (100) et l'horloge de transfert (101) est plus

lente qu'une horloge (104) pour le processeur (103), et en ce que le dispositif de gestion d'entrées de données (10) comprend en outre :

un premier circuit de synchronisation (181) pour synchroniser une sortie à partir de l'unité de maintien d'indicateurs (170) avec l'horloge de transfert (101), la sortie étant envoyée au contrôleur (110) ; et
un second circuit de synchronisation (182) pour synchroniser la sortie de l'unité de maintien d'indicateurs (170) avec l'horloge (104) pour le processeur (103).

2. Dispositif de gestion d'entrées/sorties de données (10) selon la revendication 1, dans lequel le dispositif de transfert de données (11) comprend :

un registre à décalage (140) pour convertir des données de transmission d'un format parallèle en format série et des données de réception d'un format série en format parallèle ;
un tampon de réception (150) pour maintenir temporairement les données qui ont été stockées dans le registre à décalage (140) de telle sorte qu'elles peuvent être entrées dans le processeur (103) ; et
un tampon de transmission (130) pour maintenir temporairement les données issues du processeur (103) de telle sorte qu'elles peuvent être stockées dans le registre à décalage (140), dans lequel l'unité de maintien d'indicateurs (170) maintient l'indicateur qui montre si le tampon de transmission (130) maintient les données à la transmission des données et montre également si le tampon de réception (150) maintient les données à la réception des données.

3. Dispositif de gestion d'entrées/sorties de données (10) selon la revendication 2, dans lequel le contrôleur (110) est arrangé pour gérer le registre à décalage (140) pour transmettre à et recevoir à partir de l'appareil externe (100) les données en séries, dans lequel le contrôleur (110) est arrangé :

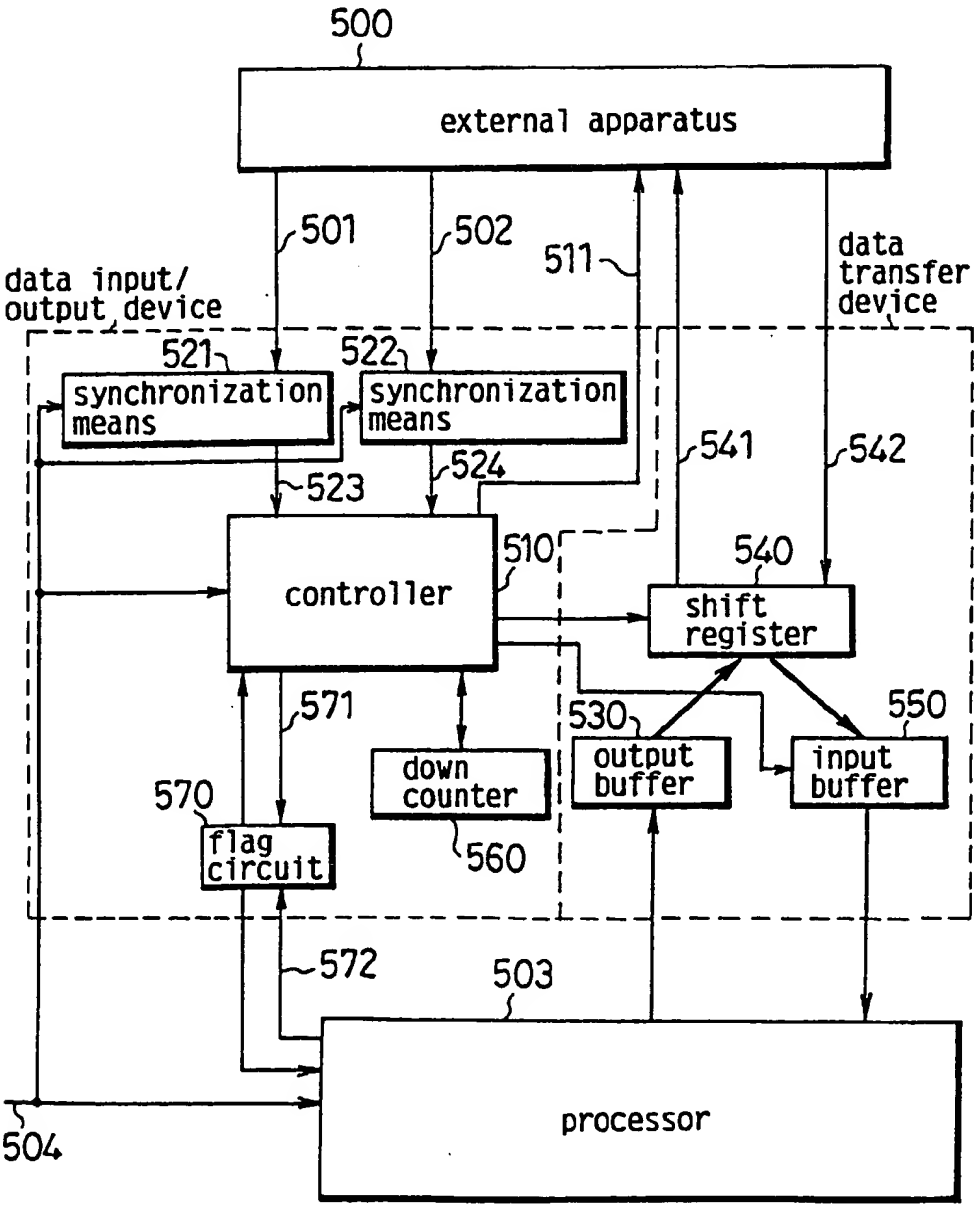
à la transmission des données, pour transférer les données dans le tampon de transmission (130) vers le registre à décalage (140) et pour délivrer une horloge de décalage (101, 211) vers le registre à décalage (140) de telle sorte que les données en séries sont transmises si l'indicateur montre que le tampon de transmission (130) maintient les données ; et
à la réception des données, pour délivrer l'horloge de décalage (101, 211) vers le registre à décalage (140) afin d'obtenir les données en séries issues de l'appareil externe (100), pour transférer les données de réception dans le registre à décalage (140) vers le tampon de réception (130), et pour changer l'indicateur dans l'unité de maintien d'indicateurs (170) pour montrer que les données de réception sont dans le tampon de réception (150).

4. Dispositif de gestion d'entrées/sorties de données (10) selon la revendication 3, dans lequel le contrôleur (110) comprend :

un circuit de contrôle de transmission (101) pour délivrer un signal de charge (212) de sorte que le registre à décalage (140) est chargé avec les données de transmission lorsque l'indicateur montre que le tampon de transmission (130) maintient les données à la transmission des données ;
un circuit de sortie d'horloge de décalage (302) pour délivrer l'horloge de décalage (101, 211) vers le registre à décalage (140) lorsque le registre à décalage (140) est chargé avec les données de transmission à la transmission des données ainsi que pour délivrer l'horloge de décalage (101, 211) vers le registre à décalage (140) lorsqu'un signal prêt à transférer est délivré par l'appareil externe (100) à la réception des données ; et
un circuit de contrôle de réception (303) pour obtenir les données de réception issues du registre à décalage (140) et changer l'indicateur dans l'unité de maintien d'indicateurs (170) pour montrer que les données de transmission y sont maintenues.

5. Dispositif de gestion d'entrées/sorties de données (10) selon l'une quelconque des revendications précédentes, comprenant en outre un compteur (160) pour compter le nombre de bits dans les données à transférer vers l'appareil externe (100) ainsi que les données en séries transférées à partir de l'appareil externe (100) vers le dispositif.

Fig. 1


500
external apparatus
501
502
511
data input/
output device
data
transfer
device
521
522
synchronization
means
synchronization
means
523
524
541
542
510
540
controller
shift
register
571
530
550
570
down
counter
output
buffer
input
buffer
flag
circuit
560
572
503
processor
504

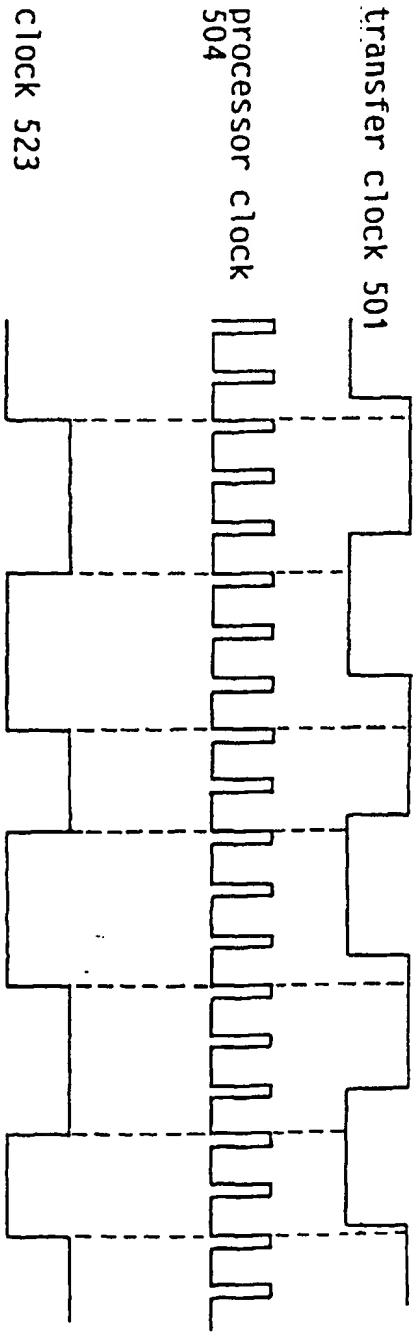


Fig. 2

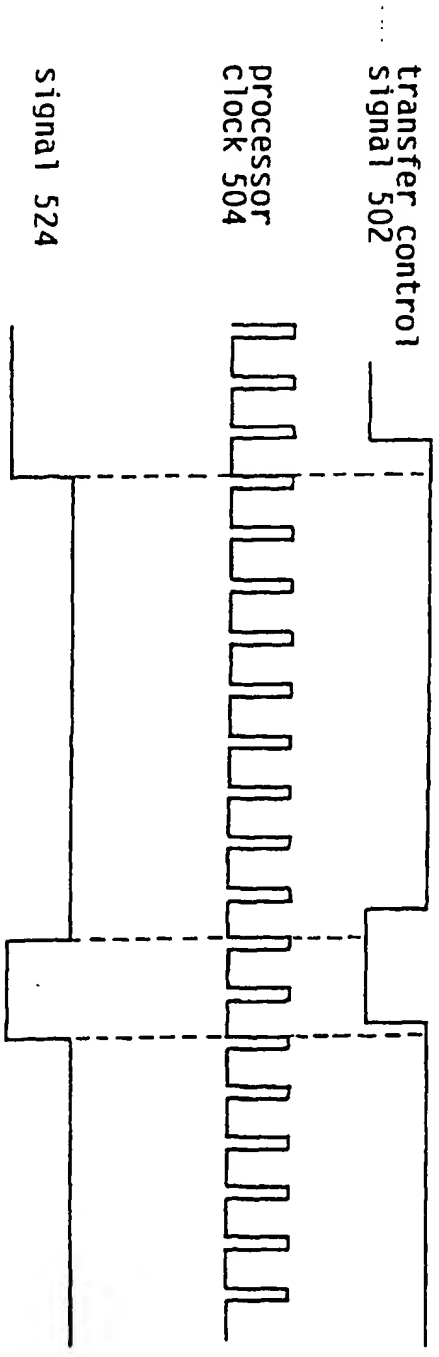
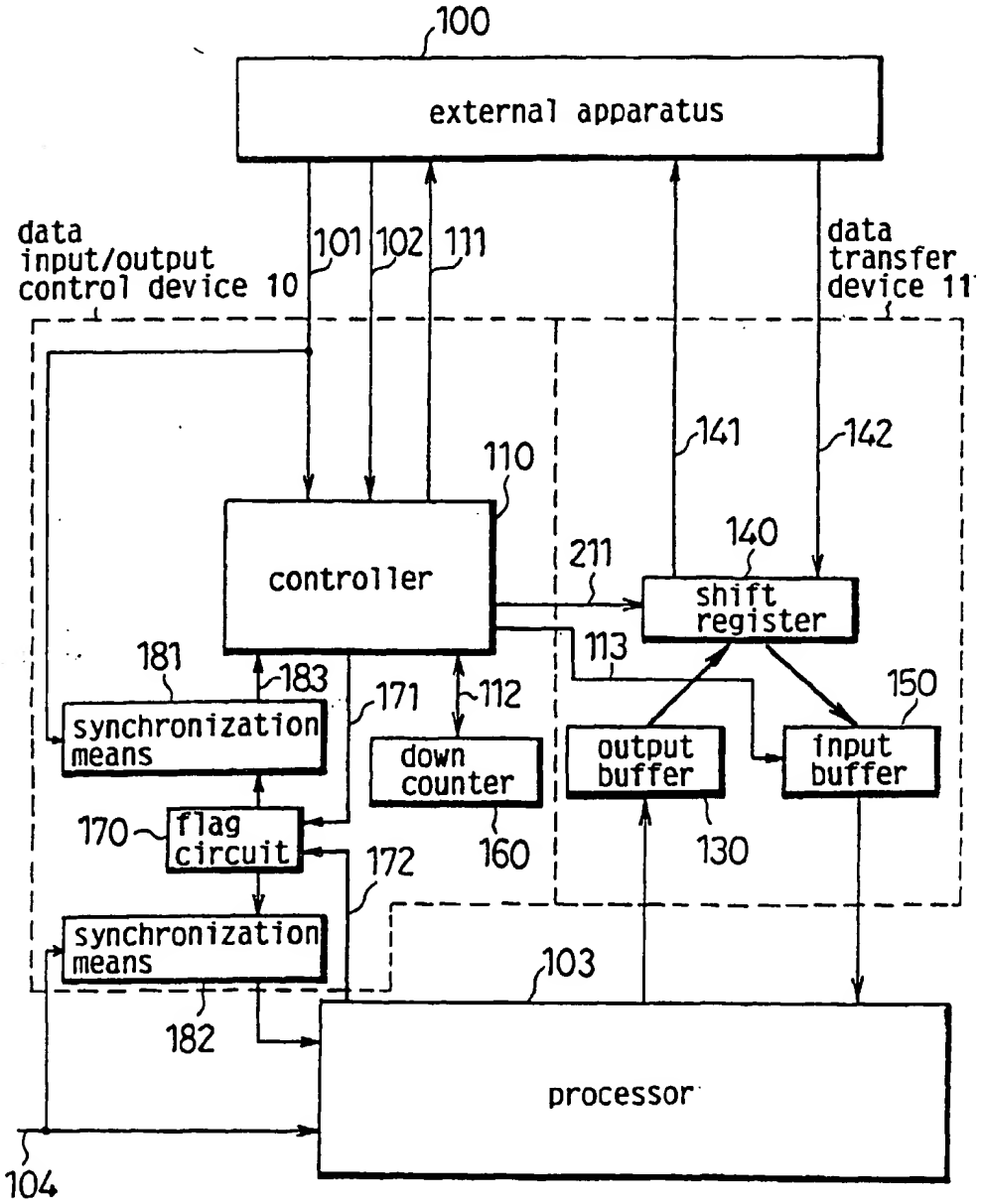

transfer control signal 502
processor clock 504
signal 524

Fig. 3

Fig. 4


100
external apparatus
data input/output control device 10
101
102
111
data transfer device 11
141
142
110
140
211
controller
shift register
113
181
183
171
112
150
synchronization means
down counter
output buffer
input buffer
170
flag circuit
160
130
172
synchronization means
103
182
processor
104

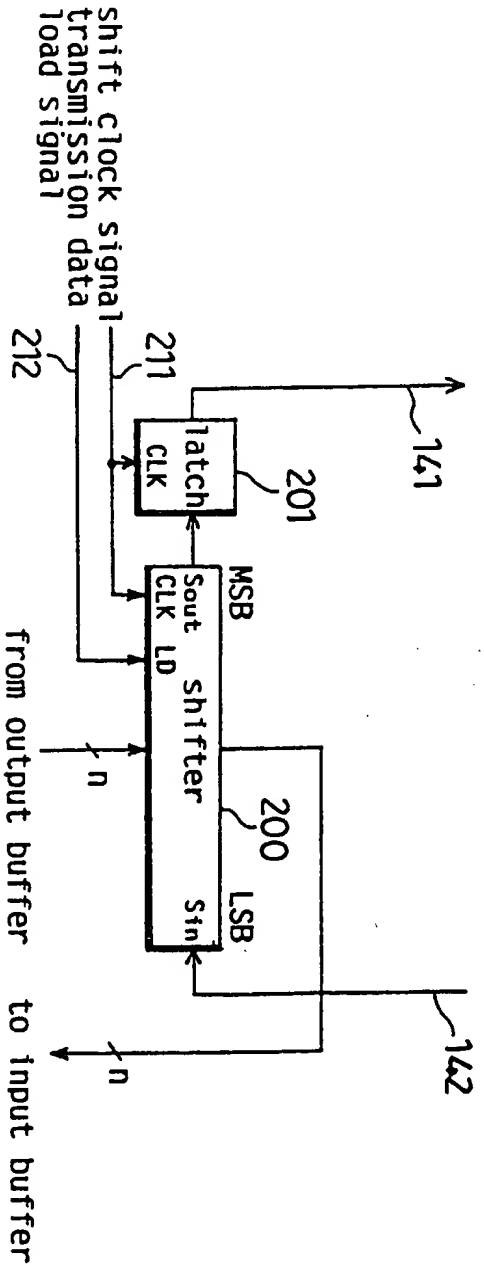

shift clock signal
transmission data
load signal
212
211
141
latch
CLK
201
MSB
Sout
CLK
LD
shifter
200
LSB
Sin
n
n
142
from output buffer
to input buffer

Fig. 5

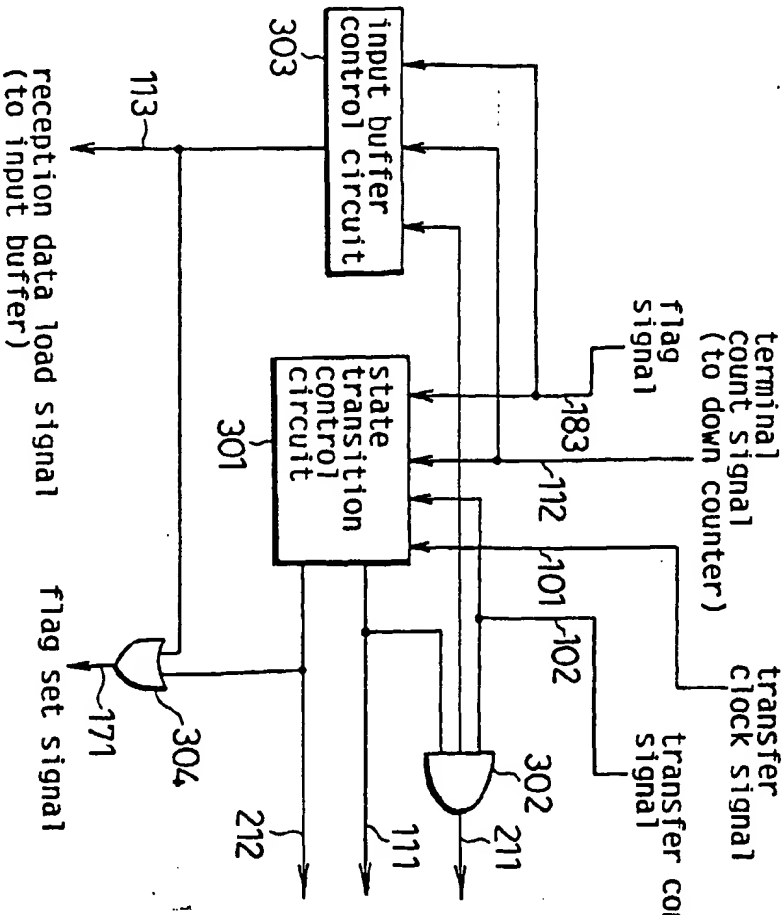

terminal count signal (to down counter)
flag signal
183
112
101
102
transfer clock signal
transfer control signal
input buffer control circuit
303
state transition control circuit
301
113
reception data load signal (to input buffer)
flag set signal
171
304
302
211
212
111
shift clock signal (to shift register)/ count clock signal (to down counter)
ready signal
transmission data load signal (to shift register)/ initial number load signal (to down counter)

Fig. 6

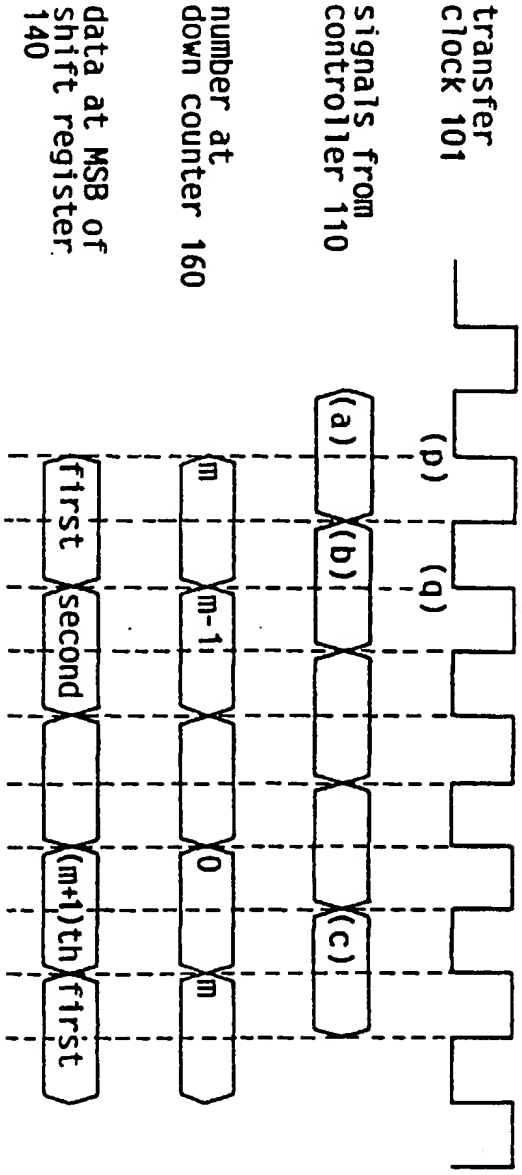

transfer clock 101
signals from controller 110
number at down counter 160
data at MSB of shift register 140
(p)
(q)
(a)
(b)
(c)
m
m-1
0
m
first
second
(m+1)th
first

Fig. 7

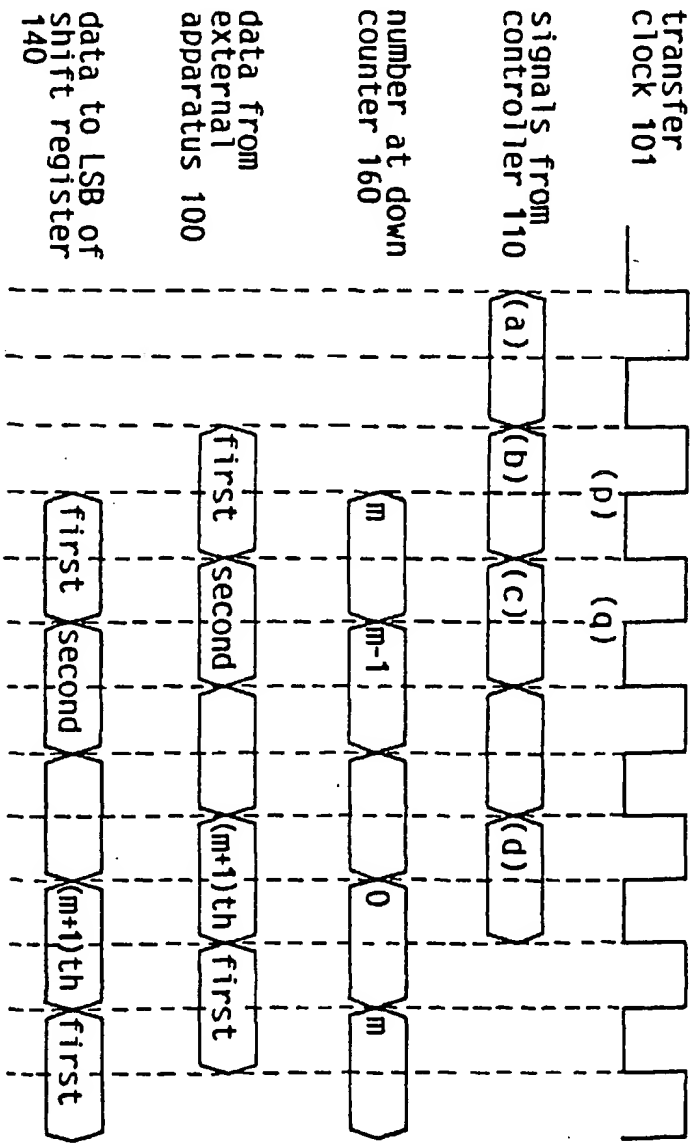

transfer clock 101
signals from controller 110
number at down counter 160
data from external apparatus 100
data to LSB of shift register 140
(a)
(b)
(c)
(d)
(p)
(q)
m
m-1
0
m
first
second
(m+1)th
first
first
second
(m+1)th
first

Fig. 8